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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/716,721	11/20/2000	Thomas Edward Horlander	RCA 89,324 / PU000125	9573

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EXAMINER	
HO, CHUONG T	

ART UNIT	PAPER NUMBER
2664	

DATE MAILED: 03/07/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/716,721	HORLANDER ET AL.	
	Examiner	Art Unit	
	CHUONG T. HO	2664	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 February 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-6,8 and 9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-6,8 and 9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Amendment filed 02/06/06 have been entered and made of record.

2. Applicant's amendment filed 02/06/06 with respect to claims 1, 3-5, 6, 8-9 have been considered but are moot in view of the new ground(s) of rejection.

3. Claims 1, 3-5, 6, 8-9 are pending.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Swenson et al. (U.S.Patent No. 5,926,120) in view of Zaun et al. (U.S.Patent No. 2002/0024610 A1).

Regarding to claim 1, see figure 1, Swenson et al. discloses all the following subject matters: a serial compressed bus interface; comprising:

- A serial-to-parallel converter (parts 21- part 28, see figure 1) having a single serial data input line (see figure 1, lines from part 11 to part 21-28; col. 3, lines 19-21) adapted to receive time-division multiplexed (11) serial data from a plurality of data sources (SI (A) – SI (H)), and having a plurality of parallel output lines (8) (see figure 1) for providing thereon a packet of time-division multiplexed

(11) serial data in parallel form to one of a plurality of devices associated with data applications ;

However, Swenson et al. is silent to disclosing Enable logic coupled to each of plurality of devices and adapted to provide at least one data valid signal that identifies each of a plurality of data consumers for which the time-division multiplexed (41) serial data is valid.

Zaun et al. discloses , see figure 1, figure 2, enable logic (IP control loci packet validation) adaped to provide at least one data valid signal that identifies which of a plurality of devices (packet buffer #1, #2, #3, #4, #5, #6) are associated with a particular packet. (see page 2, [0020], The converted data from the serial-to-parallel converter 200 is then sent to an input processor (IP) control logic block 202, which generates all of the required control and timing signals for the other processing elements in the input processor 120. One function of the IP control logic 202 is to validate input packets in the input data stream. More particularly, the IP control logic 202 extracts the PID number from the MPEG of the input packets in the 8-bit parallel data and sends the PID number to the address lines of the PID table 122 as well as a PID number buffer 203. If the PID table 122 returns a "valid" bit, either alone or with a "priority" bit if the IP control logic 202 is in a priority mode, the packet will be considered validated and send to the packet buffer 104 for storage).

Both Swenson and Zaun discloses bit select or data valid signal. Zaun recognizes enable logic adaped to provide at least one data valid signal that identifies which of a plurality of devices (packet buffer #1, #2, #3, #4, #5, #6) are associated with a particular

packet. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the system of Swenson with the teaching of Zaun to provide at least one data valid signal that identifies which of a plurality of devices are associated with a particular packet in order to re-multiplexing high speed video, audio, and data signal.

5. Regarding to claim 6, see figures 1, 3, Swenson et al. discloses all the following subject matters: a serial compressed bus interface; comprising:

- Time-division multiplexing (41) the serial compressed data from the plurality of data source (PI (0) – PI (7)) to generate time-division multiplexed serial compressed data onto a single data line (see col. 3, lines 15-21);
- Converting (parts 21-28) (see col. 2, lines 18-22) the time-division multiplexed serial data to a packet of parallel data (8, see figure 1, see col. 1, lines 15-22), and output packet of parallel data (8) for receipt by at least one of plurality of devices associated with data applications (see col. 4, lines 19-24);
- A serial-to-parallel converter (see figure 3, part 51-part 58) (see col. 2, lines 18-22) having a single serial data input line adapted to receive time-division multiplexed (41) serial data from a plurality of data sources (PI (0) – PI (7)), and having a plurality of parallel output lines (8) for providing thereon a packet of time-division multiplexed (41) serial data in parallel form (8) to one of a plurality of devices associated with data applications ;

However, Swenson et al. is silent to disclosing providing at least one data valid signal that identifies which of said plurality of devices are associated with said outputted packet of parallel data.

Zaun et al. discloses , see figure 1, figure 2, providing at least one data valid signal that identifies which of said plurality of devices (packet buffer #1, #2, #3, #4, #5, #6) are associated with said outputted packet of parallel data (see page 2, [0020], The converted data from the serial-to-parallel converter 200 is then sent to an input processor (IP) control logic block 202, which generates all of the required control and timing signals for the other processing elements in the input processor 120. One function of the IP control logic 202 is to validate input packets in the input data stream. More particularly, the IP control logic 202 extracts the PID number from the MPEG of the input packets in the 8-bit parallel data and sends the PID number to the address lines of the PID table 122 as well as a PID number buffer 203. If the PID table 122 returns a "valid" bit, either alone or with a "priority" bit if the IP control logic 202 is in a priority mode, the packet will be considered validated and send to the packet buffer 104 for storage).

Both Swenson and Zaun discloses bit select or data valid signal. Zaun recognizes providing at least one data valid signal that identifies which of said plurality of devices are associated with said outputted packet of parallel data. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the system of Swenson with the teaching of Zaun to provide at least one data valid signal

that identifies which of a plurality of devices are associated with a particular packet in order to re-multiplexing high speed video, audio, and data signal.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 3, 4, 5, 8, 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over combined system (Swenson –Zaun) in view of Pannell (U.S.Patent No. 6,636,483 B1).

In the claim 3, the combined system (Swenson – Zaun) discloses the limitations of claim 1 above.

However, the combined system (Swenson – Zaun) is silent to disclosing a a request control circuit (selector 42) adapted to output at least one request signal that requests the time-division multiplexed (41) serial data for at least one of the plurality of devices (51-58) associated with data applications

Pannell discloses a request control circuit (request control state machine 50, see figur4, col. 6, lines 21-35) adapted to output at least one request signal that requests the time-division multiplexed (multiplexer 52) serial data for at least one of the plurality of devices associated with data applications (see col. 6, lines 21-35).

Both Swenson, Zaun, and Pannell discloses the time division multiplexing, FIFO buffers. Pannell discloses a request control circuit (request control state machine 50,

see figur4, col. 6, lines 21-35) adapted to output at least one request signal that requests the time-division multiplexed (multiplexer 52) serial data for at least one of the plurality of devices associated with data applications. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the combined system (Swenson – Zaun) with the teaching of Pannell to provide a request control circuit adapted to output at least one request signal that requests the time-division multiplexed (multiplexer 52) serial data for at least one of the plurality of devices associated with data applications in order to implement a flow control system for an output buffer.

7. Regarding to claim 4, the combined system (Swenson – Zaun) discloses the limitations of claim 1 above.

However, the combined system (Swenson – Zaun) is silent to disclosing at least one encoder adapted to encode at least one of the at least one data valid signal and the at least one request signal to corresponding to more than one plurality of devices with data applications.

Pannell discloses at least one encoder adapted to encode at least one of the at least one data valid signal and the at least one request signal to corresponding to more than one plurality of devices with data applications (see col. 5, lines 62-67, As it loads packet data into FIFO buffer 32, interface circuit 30 determines from its nibble count when the data packet's source and destination fields (SRC and DEST) appear in FIFO buffer 32. At that point network interface 30 pulses a shift in signal causing a FIFO buffer 36 to store the SRC and DEST fields. When FIFO buffer 36 is not empty it

deasserts an EMPTY output signal supplied to a request control state machine 50. State machine 50 monitors the EMPTY signal and when the EMPTY signal is deasserted, and input port R0 is not currently forwarding a data packet via the V0 line, state machine 50 transmits an SO signal to FIFO buffer 36 causing it to shift out its longest stored SRC and DEST fields to a translation request generator 38. Translation request generator 38 converts the SRC and DEST fields into an encoded translation request (TRANS_REQ) and, under control of state machine 50, forwards the TRANS_REQ through a multiplexer 52 to a parallel-in, serial-out shift register 56. State machine 50 then serially shifts the translation request out of shift register 56 onto line V0. Address translator 26 of FIG. 2 monitors the V0 line for encoded translation requests, and when it detects a translation request, it reads the address information it conveys and returns an encoded translation response via line V0 to the requesting input port R0).

Both Swenson, Zaun, and Pannell discloses the time division multiplexing, FIFO buffers. Pannell recognizes at least one encoder (address 39) adapted to encode at least one of the at least one data valid signal and the at least one request signal to corresponding to more than one plurality of devices (51-58) with data applications. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the combined system (Swenson – Zaun) with the teaching of Pannell to provide at least one encoder (address 39) adapted to encode at least one of the at least one data valid signal and the at least one request signal to corresponding to

more than one plurality of devices (51-58) with data applications in order to implement a flow control system for an output buffer.

8. Regarding to claim 5, the combined system (Swenson – Zaun) discloses the limitations of claim 1 above.

However, the combined system (Swenson – Zaun) is silent to disclosing at least one encoder adapted to encode at least one of the at least one data valid signal and the at least one request signal to corresponding to more than one plurality of devices with data applications.

Pannell discloses at least one encoder adapted to encode at least one of the at least one data valid signal and the at least one request signal to corresponding to more than one plurality of devices with data applications (see col. 5, lines 62-67, As it loads packet data into FIFO buffer 32, interface circuit 30 determines from its nibble count when the data packet's source and destination fields (SRC and DEST) appear in FIFO buffer 32. At that point network interface 30 pulses a shift in signal causing a FIFO buffer 36 to store the SRC and DEST fields. When FIFO buffer 36 is not empty it deasserts an EMPTY output signal supplied to a request control state machine 50. State machine 50 monitors the EMPTY signal and when the EMPTY signal is deasserted, and input port R0 is not currently forwarding a data packet via the V0 line, state machine 50 transmits an SO signal to FIFO buffer 36 causing it to shift out its longest stored SRC and DEST fields to a translation request generator 38. Translation request generator 38 converts the SRC and DEST fields into an encoded translation request (TRANS_REQ) and, under control of state machine 50, forwards the

TRANS_REQ through a multiplexer 52 to a parallel-in, serial-out shift register 56. State machine 50 then serially shifts the translation request out of shift register 56 onto line V0. Address translator 26 of FIG. 2 monitors the V0 line for encoded translation requests, and when it detects a translation request, it reads the address information it conveys and returns an encoded translation response via line V0 to the requesting input port R0).

Both Swenson, Zaun, and Pannell discloses the time division multiplexing, FIFO buffers. Pannell recognizes at least one encoder (address 39) adapted to encode at least one of the at least one data valid signal and the at least one request signal to corresponding to more than one plurality of devices (51-58) with data applications. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the combined system (Swenson – Zaun) with the teaching of Pannell to provide at least one encoder (address 39) adapted to encode at least one of the at least one data valid signal and the at least one request signal to corresponding to more than one plurality of devices (51-58) with data applications in order to implement a flow control system for an output buffer.

9. In the claim 8, the combined system (Swenson – Zaun) discloses the limitations of claim 1 above.

However, the combined system (Swenson – Zaun) is silent to disclosing the step of encoding a data valid signal to indicate the time-division multiplexed serial compressed data is valid for more than one of devices associated with data application.

Pannell discloses the step of encoding a data valid signal to indicate the time-division multiplexed serial compressed data is valid for more than one of devices associated with data application (see col. 5, lines 62-67, As it loads packet data into FIFO buffer 32, interface circuit 30 determines from its nibble count when the data packet's source and destination fields (SRC and DEST) appear in FIFO buffer 32. At that point network interface 30 pulses a shift in signal causing a FIFO buffer 36 to store the SRC and DEST fields. When FIFO buffer 36 is not empty it deasserts an EMPTY output signal supplied to a request control state machine 50. State machine 50 monitors the EMPTY signal and when the EMPTY signal is deasserted, and input port R0 is not currently forwarding a data packet via the V0 line, state machine 50 transmits an SO signal to FIFO buffer 36 causing it to shift out its longest stored SRC and DEST fields to a translation request generator 38. Translation request generator 38 converts the SRC and DEST fields into an encoded translation request (TRANS_REQ) and, under control of state machine 50, forwards the TRANS_REQ through a multiplexer 52 to a parallel-in, serial-out shift register 56. State machine 50 then serially shifts the translation request out of shift register 56 onto line V0. Address translator 26 of FIG. 2 monitors the V0 line for encoded translation requests, and when it detects a translation request, it reads the address information it conveys and returns an encoded translation response via line V0 to the requesting input port R0).

Both Swenson, Zaun, and Pannell discloses the time division multiplexing, FIFO buffers. Pannell recognizes the step of encoding a data valid signal to indicate the time-division multiplexed serial compressed data is valid for more than one of devices

associated with data application. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the combined system (Swenson – Zaun) with the teaching of Pannell to provide the step of encoding a data valid signal to indicate the time-division multiplexed serial compressed data is valid for more than one of devices associated with data application in order to implement a flow control system for an output buffer.

10. In the claim 9, the combined system (Swenson – Zaun) discloses the limitations of claim 1 above.

However, the combined system (Swenson – Zaun) is silent to disclosing the step of encoding a request signal to indicate that the time-division multiplexed serial compressed data is requested by more than one devices associated with data applications.

Pannell discloses the step of encoding a request signal to indicate that the time-division multiplexed serial compressed data is requested by more than one devices associated with data applications (see col. 5, lines 62-67, As it loads packet data into FIFO buffer 32, interface circuit 30 determines from its nibble count when the data packet's source and destination fields (SRC and DEST) appear in FIFO buffer 32. At that point network interface 30 pulses a shift in signal causing a FIFO buffer 36 to store the SRC and DEST fields. When FIFO buffer 36 is not empty it deasserts an EMPTY output signal supplied to a request control state machine 50. State machine 50 monitors the EMPTY signal and when the EMPTY signal is deasserted, and input port R0 is not currently forwarding a data packet via the V0 line, state machine 50 transmits an SO

signal to FIFO buffer 36 causing it to shift out its longest stored SRC and DEST fields to a translation request generator 38. Translation request generator 38 converts the SRC and DEST fields into an encoded translation request (TRANS_REQ) and, under control of state machine 50, forwards the TRANS_REQ through a multiplexer 52 to a parallel-in, serial-out shift register 56. State machine 50 then serially shifts the translation request out of shift register 56 onto line V0. Address translator 26 of FIG. 2 monitors the V0 line for encoded translation requests, and when it detects a translation request, it reads the address information it conveys and returns an encoded translation response via line V0 to the requesting input port R0).

Both Swenson, Zaun, and Pannell discloses the time division multiplexing, FIFO buffers. Pannell recognizes the step of encoding a request signal to indicate that the time-division multiplexed serial compressed data is requested by more than one devices associated with data applications. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the combined system (Swenson – Zaun) with the teaching of Pannell to provide the step of encoding a request signal to indicate that the time-division multiplexed serial compressed data is requested by more than one devices associated with data applications in order to implement a flow control system for an output buffer.

Conclusion

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to CHUONG T. HO whose telephone number is (571) 272-3133. The examiner can normally be reached on 8:00 am to 4:00 pm.

The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

02/22/06

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